REMARKS

Applicant notes the filing of a Supplemental Information Disclosure Statement herein on December 27, 2000. Applicant respectfully requests that the information cited on the Form PTO-1449 be made of record herein and that the Examiner return an initialed copy of the Form PTO-1449.

The Final Office Action mailed December 21, 2000, has been received and reviewed. Claims 1, 3-10, 19 and 21-28 are currently pending in the application. Claims 1, 3-10, 19 and 21-28 stand rejected. Applicant has canceled claims 7, 8, 25, and 26. Applicant proposes to amend claims 1, 3, 9, 10, 19, 21, 27, and 28, and respectfully requests reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,986,299 to Nakamura et al.

Claims 1, 3-10, 19 and 21-28 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nakamura, et al., U.S. Patent No. 5,986,299. Applicant respectfully traverses this rejection, as hereinafter set forth.

Nakamura et al. teaches the formation of wiring as bit lines and subword lines in peripheral circuit portions of memory such as DRAM. More specifically, as illustrated in FIGS. 4, 16, and 18, the wiring layers (11, 14, 17) patterned over the insulating layer (8) facilitate the reduction of resistance between contact plugs (10, 13, 16, 19). The bit lines (11) of Nakamura et al. extend across multiple contact plugs as illustrated in FIGS. 46 through 49. *See, Nakamura et al.*, col. 9, lines 17-24. Specifically, FIG. 49 of Nakamura et al. demonstrates that bit lines (11) extend across multiple bit line contacts, or contact plugs.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant submits that presently amended independent claims 1, 3, 19, and 21 overcome the anticipation rejection based upon Nakamura et al. Specifically, presently amended claim 1 clearly claims "an individual contact land disposed atop said single contact plug." Support for this amendment is found in part in the Specification of the present application at page 15, lines 2-6 and in FIG. 16. Nakamura et al. does not explicitly or inherently disclose such a structure. Instead, Nakamura et al. only discloses bit lines which span multiple contact plugs. Such a disclosure does not anticipate amended claim 1 because the bit lines (11) of Nakamura et al. are not individual contact lands disposed over single contact plugs. The failure of Nakamura et al. to explicitly or inherently describe, in as complete detail as in claim 1, individual contact lands, precludes an anticipation rejection under 35 U.S.C. § 102(e). *See, Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Similarly, presently amended claim 19 recites "an individual contact land disposed atop said single contact plug, said individual contact land wider than said contact plug and substantially planar." As with claim 1, Nakamura et al. fails to explicitly or inherently describe an individual contact land as claimed in claim 19. This failure precludes the present anticipation rejection under 35 U.S.C. § 102(e). *See, Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Presently amended claim 3 recites "an individual drain contact land disposed atop each of said at least one drain contact plugs" and "an individual source contact land disposed atop each of said at least one source contact plugs." Nakamura et al. does not explicitly or inherently disclose individual contact lands disposed atop each of the contact plugs described by Nakamura et al. Instead, Nakamura et al. only illustrates bit lines spanning multiple contact plugs. Therefore, Nakamura et al. fails to explicitly or inherently describe each and every element of claim 3, specifically, individual drain or source contact lands disposed atop each drain or source

contact plug. The anticipation rejection under 35 U.S.C. § 102(e) is therefore improper. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Similarly, presently amended claim 21 recites "an individual drain contact land disposed atop said at least one drain contact plug" and "an individual source contact land disposed atop said at least one source contact plug." Nowhere does Nakamura et al. explicitly or inherently disclose such structures. Presently amended claim 21 recites specifically an individual source contact land and an individual drain contact land, which are not set forth in the reference relied upon for the anticipation rejection under 35 U.S.C. § 102(e). The anticipation rejection is therefore improper. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claims 4 and 22 depend from independent claims 3 and 21, respectively. As dependent claims, claims 4 and 22 incorporate the limitations of the independent claims from which they depend. Claims 3 and 21 have been amended to overcome the anticipation rejection. Claims 4 and 21, therefore, are allowable because the independent claims from which they depend are allowable.

Claims 5 through 8 and 23 through 26 also depend from amended independent claims which are now in allowable form. As such, claims 5 through 8 and 23 through 26 should also be allowed because Nakamura et al. fails to teach all of the claim limitations claimed in the independent claims from which claims 5 through 8 and 23 through 26 depend.

Claims 9, 10, 27, and 28 also depend from allowable independent claims and are therefore allowable themselves. Furthermore, presently amended claim 9 distinguishes the contact lands as "individual source contact lands" which are not explicitly or inherently disclosed in Nakamura et al. Likewise, claim 10 claims "at least one upper drain contact extends between at least two individual drain contact lands" which Nakamura et al. does not set forth. The amendments to claims 27 and 28 are similar to those of claims 9 and 10 and include the "individual source contact lands" and "individual drain contact lands" which are not explicitly or inherently described by Nakamura et al. Nakamura et al.'s failure to set forth all of the

limitations of claims 9, 10, 27, 28, and the independent claims from which those claims depend, precludes an anticipation rejection of those claims under 35 U.S.C. § 102(e). *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 3, 9, 10, 19, 21, 27, and 28 above should be entered by the Examiner because the amendments comply with the provisions of 35 U.S.C. § 132 as they are supported by the as-filed specification, drawings, original claims, and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1, 3-6, 9-10, 19, 21-24, and 27-28 are believed to be in condition for allowance, and a notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,

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APPENDIX A - Proposed Claim Amendments

1. (Three Times Amended) A contact for a semiconductor device, comprising:

a single contact plug extending through a first barrier layer, [wherein] said single contact plug [is] in electrical communication with an active region on a semiconductor substrate;

[a] an individual contact land disposed atop said single contact plug, wherein said contact land is wider than said single contact plug and is substantially planar;

an upper contact extending through a second barrier layer, [which is] said second barrier layer disposed over said first barrier layer[,] to form an electrical contact with said individual contact land.

3. (Three Times Amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one drain region and said at least one source region on said at least one active area;

a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

[at least one] an individual drain contact land disposed atop each of said at least one drain contact [plug] plugs, [wherein] said [at least one] individual drain contact land [is] wider than said at least one drain contact plug and [is] substantially planar;

[at least one] an individual source contact land disposed atop each of said at least one source contact [plug] plugs, [wherein] said [at least one] individual source contact land [is] wider than said at least one source contact plug and [is] substantially planar;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, [wherein] said at least one upper source contact is in electrical communication with at least one of said [at least one] individual source contact [land] lands; and

at least one upper drain contact extending through said second barrier layer, [wherein] said at least one upper drain contact [is] in electrical communication with at least one of said [at least one] individual drain contact [land] lands.

4. (Amended) The transistor of claim 3, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

5. (Twice Amended) The transistor of claim 3, wherein said at least one source contact plug extends between at least two source regions.

6. (Twice Amended) The transistor of claim 3, wherein said at least one drain contact plug extends between at least two drain regions.

7. (Canceled)

8. (Canceled)

9. (Three Times Amended) The transistor of claim 3, wherein said at least one upper source contact extends between at least two individual source contact lands.

10. (Three Times Amended) The transistor of claim 3, wherein said at least one upper drain contact extends between at least two individual drain contact lands.

19. (Twice Amended) A semiconductor device including at least one contact, comprising:

a single contact plug extending through a first barrier layer, [wherein] said single contact plug [is] in electrical communication with an active region on a semiconductor substrate;

[a] an individual contact land disposed atop said single contact plug, [wherein] said individual contact land [is] wider than said single contact plug and [is] substantially planar; and

an upper contact extending through a second barrier layer, [which is] said second barrier layer disposed over said first barrier layer[,] to form an electrical contact with said individual contact land.

21. (Three Times Amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

[at least one] an individual drain contact land disposed atop said at least one drain contact plug, [wherein] said [at least one] individual drain contact land [is] wider than said at least one drain contact plug;

[at least one] an individual source contact land disposed atop [a plurality of] said at least one source contact [plugs] plug, [wherein] said [at least one] individual source contact land is wider than said at least one source contact plug;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, [wherein] said at least one upper source contact [is] in electrical communication with at least one said [at least one] individual source contact land; and

at least one upper drain contact extending through said second barrier layer, [wherein] said at least one upper drain contact [is] in electrical communication with at least one said [at least one] individual drain contact land.

22. The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

23. (Amended) The semiconductor device of claim 21, wherein said at least one source contact plug extends between at least two source regions.

24. (Amended) The semiconductor device of claim 21, wherein said at least one drain contact plug extends between at least two drain regions.

25. (Canceled)

26. (Canceled)

27. (Amended) The semiconductor device of claim 21, wherein said at least one upper source contact extends between at least two individual source contact lands.

28. (Twice Amended) The semiconductor device of claim 21, wherein said at least one upper drain contact extends between at least two individual drain contact lands.